[No. of Printed Pages – 6]

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BTC/BTI/UCS-502

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B. TECH (CSE, IT), B. TECH (CSE) + MBA DUAL DEGREE & B. TECH (CSE) – EVENING

FIFTH SEMESTER END TERM EXAMINATION : NOVEMBER, 2013

COMPUTER ORGANIZATION & ARCHITECTURE

Time : 3 Hrs. *Maximum Marks : 70*

Note: ***Attempt questions from all sections as directed.***

SECTION – A (30 Marks)

Attempt any **5** *questions.*
Each question carries **6** *marks.*

1. (a) Design an arithmetic circuit with one selection variable $ and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input Carry. Draw the logic diagram for the first two stages.

$		
0	D=A+B(Add)	D=A+1(increment)
1	D=A–1(decrement)	D=A+B+1(subtract)

(b) Register A holds 8 bit binary 11011001. Determine the B operand and the logic operation to be performed in order to change the value in A to

(i) 01101101

(ii) 11111101 (2)

2. What is pipelining ? Explain the instruction pipelining with example.

3. (a) If a system uses a control memory of 1024 words of 32 bits each. The micro-instruction field has three fields (micro-operation, address, select). The micro-operation field has 16 bits.

(i) How many bits are there in branch address field and select field ?

(ii) For 16 status bits how many bits in branch logic are used to select a status bit ?

(iii) How many bits are left to select an input for MUX ?

(b) Explain how mapping from an instruction code to a microinstruction address can be done by means of a ROM. What is advantage of this method ?

4. How a Computer instruction is executed ? Draw and explain the flowchart of instruction cycle considering interrupt ?

5. (a) A digital computer has a memory unit of 64K 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

   (i) How many bits are there in the tag, index block, and word files of the address format ?

   (ii) How many bits are there in each word of cache, and how are they divided into functions ? Include a valid bit.

   (iii) How many blocks can the cache accommodate ?

   (b) Draw and explain the 4-bit by 3-bit array multiplier.

6. Explain the following Terms :

   (i) Daisy Chaining Priority Interrupt System

   (ii) Polling Process

SECTION – B (20 Marks)

Attempt any **two** *questions.*
Each question carries **10** *marks.*

7. (a) A two-word instruction is stored in memory at an address designated by the symbol W. The address field of the instruction (stored at W+1) is designated by the symbol Y. The operand used during the execution of the instruction is stored at an address symbolized by Z. An index register contains the value X. State how Z is calculated from the other addresses if the addressing mode of the instruction is

(i) Direct

(ii) Indirect

(iii) Relative

(iv) Indexed (8)

(b) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speed up that can be achieved? (2)

8. (a) Explain Virtual Memory. Also show the implementation of Page Table. (6)

(b) A virtual memory system has an address space of 8k words, a memory space of 4k words, and page and block sizes of 1k words. The following page reference changes occur during a given time interval.

4 2 0 1 2 6 1 4 0 1 0 2 3 5 7

Determine the four pages that are resident in main memory after each page reference change if the replacement algorithm used is

(i) FIFO

(ii) LRU (4)

9. Differentiate between the following :

(a) RICS and CISC

(b) Hardwired Control Unit and Micro-programmed Control Unit

(c) BUN and BSA

SECTION – C (20 Marks)

(Compulsory)

10. (a) Show the contents of registers E.A.Q, and SC during the process of division of 10100011 by 1011. (8)

(b) Why are the read and write control lines in a DMA controller bidirectional? Under what condition and for what purpose are they used as inputs? Under what condition and for what purpose are they used as outputs? (3)

(c) Differentiate between the Isolated I/O and Memory Mapped I/O. (6)

(d) How many times does the control unit refer to memory when it fetches and executes an indirect addressing model instruction if the instruction is

(i) A computational type requiring an operand from memory

(ii) A branch type (3)